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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,500	04/23/2001	Roger S. Tsai	12-1128	4458

27160 7590 07/12/2006

PATENT ADMINISTRATOR
KATTEN MUCHIN ROSENMAN LLP
1025 THOMAS JEFFERSON STREET, N.W.
EAST LOBBY: SUITE 700
WASHINGTON, DC 20007-5201

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,500	TSAI, ROGER S.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 were examined.

Section I: Reopening Prosecution

2. In view of the appeal brief filed on 03/27/2006 PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options: (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2). Reopening is necessitated based on applicants' argument in the brief. Based on applicants' brief and interpretation, examiner has provided new art and looks forward to advancing prosecution.

Section II: Non-Final Rejection

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh et al., (US Patent 5,878,053; hereafter Koh) in view of Pfeifer et al., titled, "Fabrication and Characterization of Freely Positionable Silicon-On-Sapphire Photoconductive Probes" (hereafter Pfeifer). Koh teaches a method for analyzing a semiconductor chip design for determining potential voltage drop and electromigration problems (abstract); but doesn't teach fabrication using a scanning electron microscope.

Pfeifer teaches fabrication of photoconductive probes on silicon-on-sapphire (abstract) using S-parameter measurements (Introduction, left column, 2nd paragraph, lines 3-4) with a scanning electron microscope (pg. 2548, left column, lines 11-12).

Koh and Pfeifer are analogous art since they teach semiconductor design and fabrication.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the method of fabricating positionable PC probes of Pfeifer in the reliability analysis tool to test and simulate the power network of submicron IC designs of Koh since Pfeifer teaches a method by which the time

resolution can be improved by optimized ion implantation (Pfeifer: pg. 2552, "Conclusion" section, lines 6-7).

Claim 1. A method for modeling one or more predetermined characteristics of a semiconductor (Koh: abstract) device comprising the steps: a) fabricating (Pfeifer: abstract) a semiconductor (Koh: abstract) device; b) measuring ("measuring modern electronic devices" Pfeifer: pg. 2547, Introduction, left column, 2nd paragraph, line 4)) one or more predetermined physical characteristics of said semiconductor (Koh: abstract) device; c) testing the semiconductor (Koh: abstract and Pfeifer: pg.2547, right column, line 5) device; to establish a physically representative equivalent model (Koh: abstract) of said one or more characteristics of said semiconductor (Koh: abstract) device; d) varying one or more of said predetermined physical characteristics and fabricating (Pfeifer: abstract) a subsequent (Koh: column 5, lines 4-5) semiconductor (Koh: abstract) device with said varied dimensions (examples of various dimensions, Pfeifer: pg.2547, figures 1 and 2); and e) testing of the sample ("test wafer" Pfeifer: pg. 2548, left column, line 12) to a establish a correct said physically representative model.

Claim 2. The method as recited in claim 1, further including the step of measuring ("measuring modern electronic devices" Pfeifer: pg. 2547, Introduction, left column, 2nd paragraph, line 4)) the varied dimensions (examples of various dimensions, Pfeifer: pg.2547, figures 1 and 2) after said subsequent semiconductor (Koh: column 5, lines 4-5) is fabricated.

Claim 3. The method as recited in claim 1, wherein a scanning electron microscope (SEM) (Pfeifer: pg. 2548, left column, line 11) is used to measure said predetermined dimensions in step (b).

Claim 4. The method as recited in claim 1, wherein said testing in step (c) includes taking S-parameter measurements (Pfeifer: pg. 2548, left column, line 11) of said semiconductor (Koh: abstract) device.

Claim 6. The method as recited in claim 1, wherein said one or more predetermined physical characteristics include the physical dimensions (examples of various dimensions, Pfeifer: pg.2547, figures 1 and 2) of the source access region of said semiconductor (Koh: abstract) device.

Claim 7. The method as recited in claim 1, wherein said varied dimensions (examples of various dimensions, Pfeifer: pg.2547, figures 1 and 2) are measured by way of a SEM (Pfeifer: pg. 2548, left column, line 11).

Claim 8. The method as recited in claim 1, wherein said corrected physically representative model is corrected based upon S-parameter measurements (Pfeifer: pg. 2548, left column, line 11).

Claim 9. A process for making a semiconductor (Koh: abstract) device comprising the steps of: a) fabricating (Pfeifer: abstract) a semiconductor (Koh: abstract) device; b) measuring ("measuring modern electronic devices" Pfeifer: pg. 2547, Introduction, left column, 2nd paragraph, line 4))one or more predetermined physical characteristics defining measured characteristics of said semiconductor (Koh: abstract) device; c) testing said semiconductor (Koh: abstract) device to establish a physically representative model; d) fabricating (Pfeifer: abstract) a subsequent semiconductor (Koh: column 5, lines 4-5) device in which said one or more measured characteristics are varied; defining varied characteristics. e) measuring ("measuring modern electronic devices" Pfeifer: pg. 2547, Introduction, left column, 2nd paragraph, line 4)) said varied characteristics; and f) testing said semiconductor (Koh: abstract) device to establish a revised physically representative model of said semiconductor (Koh: abstract) device.

Claim 10. The process as recited in claim 9, further including step (g) repeating steps (d) through (f) one or more times (at user's discretion).

Claim 11. The process as recited in claim 9, wherein said physically representative model in steps (c) and (b) is based on predetermined S-parameter measurements (Pfeifer: pg. 2548, left column, line 11).

Claim 12. The process as recited in claim 9, wherein steps (b) and (e) include

measurement by way of a scanning electron microscope (Pfeifer: pg. 2548, left column, line 11).

6. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Koh as modified by Pfeifer as applied to claim 1 above, and further in view of Ishimaru et al., titled "Mechanical Stress Induced MOSFET Punch-through and Process Optimization for Deep Submicron TEOS-O3 Filled STI Device" (hereafter Ishimaru).

Koh as modified by Pfeifer teaches most of the instant invention as applied to claim 1 above; however, Koh as modified by Pfeifer, fails to teach semiconductor process, scaling, bias, temperature and device layout.

Ishimaru teaches the mechanical stress simulation of a MOSFET (title with pg.123, left column, 2nd paragraph, line 1).

Koh as modified by Pfeifer with Ishimaru are analogous since they teach semiconductor fabrication.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize stress simulation procedure of Ishimaru in the semiconductor design process of Koh as modified by Pfeifer since Ishimaru teaches a method of scaling down the shallow trench (STI) device dimensions for achieving lower mechanical stress and higher manufacturability (Ishimaru: pg. 123, right column, "Process Optimization" section, lines 20-23).

Claim 5. The method as recited in claim 1, wherein said one or more predetermined characteristics include device scaling (Ishimaru: pg. 123, right column, "Process Optimization" section, lines 20-23); bias dependence (Ishimaru: pg. 124 figure 2b "Reverse Bias"); temperature(Ishimaru: pg. 124 figures 5 and 6) dependence; lay out (Ishimaru: pg. 123, right column, 2nd paragraph, line 15) dependence and process (Ishimaru: title and Introduction, left column, 1st paragraph, line 9) dependence.

Section III: Response to Arguments (Appeal Brief)

102/103

7. Applicant's arguments, see pages 2-8, filed 03/27/2006 with respect to the rejection(s) of claim(s) 1-4, 7-12 and 5 under 102(b) and 103(a), respectively, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Koh, Pfeifer and Ishimaru.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

June 29, 2006

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

7/6/06

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